Versatile Computing Systems

VCompS-1001 cSoC Development Environment (CDE)

Cost effective and flexible way to develop open avionics applications in a lab environment.

Application Development

- The cSoC Development Environment (CDE) is a low cost development platform that allows users to create applications for GE's open avionics platform systems powered by the GE cSoC processor

Design Assurance Documents

- CDE can be used to generate DO-178C artifacts for software applications of all criticalities (DAL A to DAL E)

Flexible interfaces

- CDE provides standard interfaces to high speed networking capabilities via ARINC-664P7, GB Ethernet, Time Sensitive Networking (TSN), and PCIe to facilitate architecture studies and lab integration

geaviation.com/systems/avionics

Product Characteristics

External Interfaces

- Interface to power the unit from 120V AC.
- Switch to control power to the CDE
- Control Buttons for System and Power on Reset's for Lane 0 and Lane 1
- LED's to display the following discrete signals:
  - Lane 0 System Ready
  - Lane 1 System Ready
  - Lane 0 BIST Enable
  - Lane 1 BIST Enable
  - Power Supply Health
  - Lockstep
  - Lab Mode
  - Platform Speed Select
- 1x JTAG interface for Lane 0 and Lane 1 (2 total)
- 1x RS-232 interface for Lane 0 and Lane 1 (2 total)
- 1x USB interface to support access to Lane 0 and Lane 1 UART interfaces (single USB interface provides access to two UART channels per lane – 4 total)
- 1x USB interface for programmable logic device interface
- 1x Thunderbolt interface for Lane 0 and Lane 1 PCIe interfaces (2 total)
- 4x Ethernet channels for Lane 0 and Lane 1 ARINC-664/ Ethernet interfaces (8 total)

Internal Interfaces

- When the lid is removed, the CDE provides the following:
  - 1x SPI for Lane 0 and Lane 1 (2 total)
  - 1x Parallel Bus for Lane 0 and Lane 1 (2 total)
  - 1x I2C for Lane 0 and Lane 1 (2 total)
  - Corner Balls connections for Lane 0 and Lane 1 (2 total)
  - 1x PCIe x4 card slot for Lane 0 and Lane 1 (2 total)
  - 2x I2C for Lane 0 and Lane 1 (4 total)
  - Corner Balls connection for Lane 0 and Lane 1 (4 total)
  - GPIO for Lane 0 and Lane 1 (16 total)

Functional and Programmability

- Programmable microcontroller for power sequencing
- Programmable logic device to externally exercise cSoC discrete interfaces
- Capability to switch between Thunderbolt and x4 Card Slots for PCIe Operation
- Capability to remove power to Lane 1
- cSoC device current and voltage monitoring
- Memory compliment
  - 4.5 GB DDR4 Memory for Lane 0 and Lane 1 Main DDR (9 GB Total)
    - 4 GB Data per Lane (8 GB Total)
    - 0.5 GB ECC per Lane (1 GB Total)
  - 4.5 GB DDR4 Memory for Lane 0 and Lane 1 IO DDR (9 GB Total)
    - 4 GB Data per Lane (8 GB Total)
    - 0.5 GB ECC per Lane (1 GB Total)
  - 4 GB ONFI 2.1 Memory for Lane 0 and Lane 1 NAND (8 GB Total)

Feature	Attribute
Size (L x W x H)	8.25 inches x 10.00 inches x 2 inches 20.9 cm x 25.4 cm x 5.1 cm
Power	Input: 115 - 220 volts AC Consumption: XX - YY watts

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